

reacting a second reactant species with the first material to leave no more than about one monolayer of a second material.

*29* 30. (Amended) A method of forming a dielectric layer having a dielectric constant greater than about 10 directly over a textured silicon bottom electrode having a hemispherical grain (HSG) morphology in an integrated circuit, comprising:

*C2* forming no more than about one monolayer of a metal-containing species in a self-limited reaction; and

reacting an oxygen-containing species with the monolayer.

*33* 35. (Amended) A process of forming a capacitor dielectric having a dielectric constant of about 10 over a hemispherical grain silicon surface, comprising:

*C3* directly coating the hemispherical grain silicon surface with no more than about one monolayer of a ligand-terminated metal complex in a first phase;

replacing ligands of the ligand-terminated metal with oxygen in a second phase distinct from the first phase; and

repeating the first and second phases in at least about 10 cycles.

*41* 63. (Amended) A method of forming a capacitor with high surface area in an integrated circuit, comprising:

*C4* forming a bottom electrode in a three-dimensional folding shape;

superimposing a hemispherical grain silicon layer over the three-dimensional folding shape; and

depositing a high k dielectric layer conformally directly over the textured morphology by cyclically supplying at least two alternating, self-terminating chemistries,  
*the layer forming part of the capacitor.*

## REMARKS

### I. Amendments

Applicants have amended Claims 1, 30, 55, and 63 to facilitate prosecution and to better protect the subject matter Applicants regard as the invention. After entry of the amendments, each of the pending claims recites an ALD-type process for depositing high-k material over an HSG morphology. Accordingly, Applicants submit that Claims 1, 3-30, 33-35 and 55-63 (the